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(56) Opposing documents:

EP 07 97 258 A2
EP 05 53 852 A2

The following specifications are taken from the documents filed by the applicant

Request for examination has been filed according to § 44 of the Patent Act

(54) Process for the production of crystalline semiconductor layers

(57) A process for the production of a crystalline semiconductor layer (26) consists in the fact that at least one porous layer (21, 31) is produced at the surface of a semiconductor substrate (20, 30) and then the porous layer is removed from the semiconductor substrate and either before or after its removal is at least partially recrystallized by heat treatment.

[see source for figure]

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Description

The invention relates to a process for the production of crystalline semiconductor layers according to claim 1.

For electronic components such as, for example, thin-layer transistors or thin-layer solar cells, thin semiconductor layers with low defect density and high diffusion length or charge carrier mobility are needed. Above all in solar cells, however, it is of significant advantage in this application if the photoactive semiconductor layers can be applied to foreign substrates such as glass or plastic. However, in the deposition of crystalline semiconductor layers on such foreign substrates epitactic growth is not possible in general. The growth thus leads to the formation of polycrystalline layers whose properties are affected by the presence of grain boundaries. For use as electronic or optoelectronic components this is usually disadvantageous.

In order to solve this problem, a series of different technologies have been proposed and applied according to the state of the art.

The simplest approach consists in mechanically sawing crystalline blocks or rods of monocrystalline semiconductor material, as described, for example, in the publication of J. Dietl et al. in "Crystals: Growth, Properties and Applications," page 73, volume 8, Springer Verlag, 1982. However, the minimum layer thicknesses which can be obtained with this process at present lie in the range of approximately 130 µm. In addition, a great problem is the very high loss in saw cuts.

Through a process designated as edge-defined film-fed growth (EFG) and described in the publication of F. V. Wald in "Crystals: Growth, Properties and Applications," page 157, volume 5, Springer Verlag, 1981 a very thin silicon foil can be produced. With this process, losses in saw cuts can in fact be avoided, but the thickness of the foils at present is typically 300 µm. It has previously still not been possible to reduce the minimum thickness which can be obtained to approximately 100 µm. The production of semi-transparent silicon layers, such as are needed for applications in displays, is not possible with this process.

The recrystallization of amorphous or polycrystalline silicon layers deposited on foreign substrates by means of a laser beam or the like has, on the one hand, proved complex and, on the other hand, turned out to be unsatisfactory in throughput.

In the so-called Smart Cut process, as, for example, is described in US-PS 5,714,395 ions are implanted in semiconductor wafers in such a manner that microblisters form in the semiconductor wafer at a certain depth predefined by the implantation parameters. Then a second semiconductor wafer is bonded to the surface of the first semiconductor wafer. Due to subsequent thermal expansion the microblisters in the first semiconductor wafer grow together to form a separation or cleavage surface. At this separation surface the second semiconductor wafer and the bonded layer of the first semiconductor wafer can be separated easily. However, due to the ion implantation this process is too expensive for low-cost applications.

Finally, a process is known from EPA 0 797 258 in which porous silicon material is used. In this process a porous layer is first produced in the surface of a first semiconductor wafer by anodic etching. A separation or cleavage surface is subsequently produced in the porous silicon layer by the growing together of pores at a certain depth due to thermal expansion. Simultaneously, the surface of the porous silicon layer is recrystallized so that on it a crystalline silicon layer can be grown epitactically. To this epitactic layer an arbitrary foreign substrate is then bonded which can be separated at the separation layer of the porous silicon. This process does indeed show relatively good exploitation of material but, due to the fact that an epitaxy step must be introduced, is technologically very complex.

For the production of electronic components, in particular solar cells, the traditional processes are thus either disadvantageous due to the layer thicknesses which can be obtained or very complex due to their technology and thus also associated with high costs.

Consequently, the objective of the present invention is to specify a process for the production of sufficiently thin, crystalline, quasicrystalline, or quasimonocrystalline semiconductor layers, said process comprising a smaller number of process steps, thus being technologically less complex, and making possible an economical manufacture of electronic and optoelectronic components on the basis of semiconductor layers.

This process is realized according to the invention by the process steps of claim 1. In the process according to the invention, at least one porous layer is produced in the semiconductor material at the surface of a semiconductor substrate. Then the porous layer is removed from the semiconductor substrate and either before or after its removal at least partially recrystallized by heat treatment. In contrast to EPA 0 797 258 the porous silicon layer is thus not used as a sacrificial layer. Rather, from it, through heat treatment, a crystalline semiconductor layer is produced which can be used in an electronic or optoelectronic component as an active layer.

According to the invention, this can be done in two different types of embodiment.

According to a first type of embodiment, the process according to the invention comprises the following process steps:

a) providing a semiconductor substrate with a surface,
b) producing a first porous layer adjacent to the surface and with a first porosity curve in a range of relatively low porosity,
c) producing a second porous layer within or adjacent to the first porous layer and with a second porosity curve which at least partially lies in a range of relatively high porosity,
d) heat-treating, and thus at least partial recrystallizing, of the first porous layer and converting at least a part of the second porous layer into a separation layer,
e) removing the first porous layer at the separation layer.

According to a second type of embodiment, the process according to the invention comprises the following process steps:

a) providing a semiconductor substrate with a surface,
b) producing a first porous layer adjacent to the surface and with a first porosity curve in a range of relatively low porosity,
c) producing a second porous layer within the, or adjacent to the, first porous layer and with a second porosity curve which is constituted in such a manner that a full-surface removal of the porous layers occurs during the process,
d) heat-treating, and thus at least partial recrystallizing, the porous layers.

Additional advantageous developments of the process according to the invention are specified in the subordinate claims.

In particular, the production of the porous silicon can be done by anodic etching, in which, for example, a two-chamber etching cell is used and solutions containing hydrogen fluoride are used.

With the process according to the invention crystalline, quasicrystalline, or quasimonocrystalline semiconductor layers with layer thickness adjustable from sub-µm to tens of µm can be applied to arbitrary substrates and can be used as the active layer of electronic or optoelectronic components, in particular solar cells. For use as the active layer of a solar cell it can prove to be advantageous that voids have remained in the recrystallized layer, said voids acting as light-scattering centers and thus increasing light absorption. The inner surfaces formed by these voids can in addition, for example, be passivized by a hydrogen fluoride treatment, by a local field (high doping at the surface), by a thin oxide layer, by introducing stable charges, or by inversion layers.

In the following, embodiment examples of the invention are described in more detail in connection with the drawings.

Shown are:

Figure 1: a two-chamber etching cell used for the process according to the invention,

Figure 2A: 2A to F, the individual stages of a production process according to a first type of embodiment of the present invention,

Figure 3A: 3A to D, the individual stages of a production process according to a second type of embodiment of the present invention,

Figure 4: the absorption coefficient of crystalline silicon layer produced according to the invention (measured experimentally) and of crystalline silicon (literature).

In **figure** 1 a two-chamber etching cell **10** known per se is represented, as can be used, for example, for the production of porous silicon. The cell consists of two chambers **1** and **2** which are spatially separated from one another by the semiconductor wafer **4** to be processed. The semiconductor wafer **4** is clamped into the cell using a sealing ring **9** so as to be liquid-tight. In the chamber **2** a hydrogen fluoride/ethanol etching solution **8** is located, while the chamber **1** is filled with a contact electrolyte **9**, such as, for example, H_2SO_4. Into the liquids of both chambers electrodes **5** and **6**, e. g., of platinum, are immersed, said electrodes being connected to the poles of a current source **3**. A surface of the semiconductor wafer **4**, specifically the surface to be processed, is facing the cathode **6**. With the current source **3** a current density in the range of 1-300 mA/cm^2 can be achieved. The temperature can lie in a range of approximately -20° C to 80° C. Typically it lies at room temperature.

In the following, a first type of embodiment is explained in more detail with the aid of **figures** 2A to F. As the semiconductor, silicon is used.

First, a suitable monocrystalline or polycrystalline silicon substrate is prepared according to **figure** 2A. As substrate material n-type silicon as well as p-type silicon come into consideration. The orientation plays no decisive role here. The starting material can be rough-sawn, textured, or polished, depending on the application.

Then, a first porous surface layer **21** is produced, in a manner known per se, by anodic etching in a two-chamber system described in **figure 1** (**figure** 2B). The layer **21** can either have a spatially constant, relatively low porosity or a porosity curve in a range of relatively low porosity over its depth. The hydrogen fluoride concentration must be relatively high to achieve low porosity, i.e. in a range of 5-50%, e. g. 37%. The current density is set in a range of 1-30 mA/cm^2 to achieve low porosity. The layer thickness is determined by the etching time. With a

current density of, for example, 12 mA/cm^2, a porous layer with a thickness of ca. 10 µm and a porosity of ca. 20 to 30% arises in 10 minutes.

According to figure 2C a second relatively thin porous layer **22** is then produced in a second etching step. This layer can have a spatially constant, relatively high porosity or a porosity curve in a range of relatively high porosity. In a preferred form of embodiment a porosity curve is produced by this etching step being carried out with a time-dependent current density. In experiments, very good results were achieved with a current ramp in which, with a hydrogen fluoride concentration of 37%, the current density was first increased in 10 seconds from 12 mA/cm^2 to 50 mA/cm^2, then held constant at 50 mA/cm^2 for 10 seconds, and finally was decreased to zero in 10 seconds. With this process control the second porous layer **22** can be formed at the boundary surface between the first porous layer **21** and the crystalline substrate **20** with a layer thickness of 50-100 nm. Corresponding to the current profile the porosity of the second porous layer **22** has a depth-dependent curve. Beginning at the boundary surface, the porosity first increases slowly, then remains over a narrow range of depth at a constant and relatively high level, and following that slowly decreases once again. If, due to the initially relatively low current, the porosity increases with depth, the resistance of the layer just produced also increases. The higher this resistance is, the better the layers lying thereover are passivized against the etching attack, whereby the second porous layer **22** is produced at the depth of the boundary surface between the first porous layer **21** and the crystalline substrate **20**.

The production of the second porous layer **22** can also be carried out, as, for example, described in EPA 0 797 258, with a time-independent current. In so doing, for example, the etching time can be set to a few seconds, e. g. between 2 and 3 seconds, and the current density to a constant value in a range between 60 and 200 mA/cm^2. With this, a porous layer **22** arises with a thickness of 50-100 nm and with a depth-independent porosity which is at least greater than that of the first layer **21**. With the choice of a relatively low current density, such as, for example, 60 mA/cm^2, the porous separation layer arises at the boundary surface to the crystalline substrate if a relatively high hydrogen fluoride concentration is present, while with the choice of a relatively high current density, such as, for example, 200 mA/cm^2, and a comparatively low hydrogen fluoride concentration, the porous separation layer is formed in the middle of the first porous layer **21**.

It is generally advantageous if the second porous layer **22** is formed on the boundary surface between the first porous layer **21** and the crystalline substrate **20** since in this case, as is still to be seen, after removing the layers the substrate does not have to be treated further, in an expensive manner, by polishing etc. and in addition the material is exploited in an optimal manner.

After completion of the etching processes the silicon wafer is removed from the two-chamber cell. The handling of the layer is simplified by the fact that the first porous layer **21** is fixed from below by the second porous layer **22** in such a manner that it is stable. Sufficient stability of the layer **22** is ensured in the above-described production by the etching parameters. The porous layers are connected to the wafer at the edge which is not etched and are fixed thereby in addition.

The now following thermal treatment of the sample can be carried out in an annealing furnace or RTP (rapid thermal processing) furnace by the action of a laser beam or by the coupling of electromagnetic radiation. When carrying out the heat treatment in a vacuum or in a protective gas (for example, Ar, He, H, or N_2 or a mixture of various protective gases), the temperatures typically lie in a range of ca. 600° C up to below the melting point of crystalline silicon. Typical parameters are a temperature of 1050° C and a duration of 2 hours under vacuum conditions. Preferably, the pore walls of the sample should be completely freed of oxide and hydrogen-terminated before the expansion process. This occurs, for example, through etching in aqueous hydrogen fluoride solutions, where a renewed oxidation has to be prevented by the process atmosphere.

The heat treatment has essentially two things as a consequence.

On the one hand, atoms move, for reasons of energy, from strongly porous materials in the direction of less strongly porous materials, that is, the atoms migrate from the strongly porous layer **22** into the weakly porous layer **21** as well as to the crystalline substrate **20** while retaining the crystal orientation. Merely a thin separation layer **23** (figure 2E) remains, which consists only of very thin fragile links, at which the weakly porous layer **21** is held in the manner of a tear-away seal on the substrate **20**. The separation layer **23** thus serves as a theoretical line of breakage to separate the substrate from the layer **21** lying thereover after the annealing process.

On the other hand, the heat treatment causes the weakly porous layer **21** to recrystallize at least partially. This means that independently of the thickness of the layer the pores on the surface regenerate nearly completely so that a cohesive surface arises. With very thin layers (up to ca. 1 µm) the recrystallization also occurs completely in volume. With greater thicknesses, to avoid voids it is necessary to also produce a porosity gradient in the first porous layer **21**. This has as a consequence the fact that the regeneration process in the temperature

treatment is done in a directed manner, whereby voids can be completely regenerated.

After the temperature treatment the recrystallized layer **26** can be separated at the separation layer **23**. For this purpose, for example, according to **figure** 2F a substrate **25** can be applied to the surface of the sample by securing with an adhesive or bonding. On one side, the substrate **25** can be an auxiliary substrate or a desirable foreign substrate of glass, plastic, or the like which should be provided with a crystalline silicon layer. After the application, the substrate **25** can be lifted off along with the recrystallized layer **26**.

Alternatively thereto, the substrate **25** can also be applied before the annealing step.

Thereafter, the silicon substrate can be used again with or without preparation (for example, polishing) for the production of additional layers. Polishing of the surface between the cycles reduces the roughness of the monocrystalline layers.

In the following a second type of embodiment is explained in more detail with the aid of **figures** 3A to F.

In **figures** 3A, B it is shown how, on a monocrystalline silicon substrate **30**, a first porous layer **31** of relatively low porosity is produced. This process step can be done as in the first type of embodiment. Reference is thus made to **figure** 2A, B and the corresponding description.

In the following the weakly porous silicon layer will be removed over its full surface by the etching process. For this, a layer **32** is formed by changing the etching parameters for a short time (**figure** 3C), said layer having a relatively high porosity. In contrast to the first type of embodiment the etching parameters are changed during the formation of the layer **32** so that the weakly porous layer **31** is removed over its full surface during the etching process (**figure** 3D).

For this, there are basically two possibilities. For one, a very high current density can be set, typically in the range of 100-300 mA/cm^2, depending, among other things, on the hydrogen fluoride concentration set. However, the etching solution can be exchanged for another with lower (1-20%) hydrogen fluoride concentration, the replacing solution producing a higher porosity at the same current density.

For example, to remove the layer with a concentration of 13.5%, the current density can be run up through a ramp in ca. 15 seconds to 160 mA/cm^2 and held at this level for ca. 5 seconds.

In the last step the removed layer **31** must be subjected to another heat treatment with the goal of its recrystallization. With regard to this, reference is made to the corresponding discussions with regard to **figure** 2E of the first type of embodiment.

The etching process can likewise be carried out with a single-chamber etching cell, in which the anode is formed by the semiconductor wafer.

It has been determined experimentally that the crystalline silicon layers produced according to the invention have an increased light absorption vis-à-vis crystalline silicon starting material. In **figure** 4 the absorption curve of a 4-µm-thick silicon layer produced according to the invention is represented in comparison to the absorption curve of customary crystalline silicon. It is shown that the silicon layer produced according to the invention has clearly higher light absorption over almost the entire visible spectral range. The explanation for this is that the enclosed voids remaining in the material act as very effective light-scattering centers. They have thus the same effect as a textured surface, which also makes possible a better luminous efficiency by multiple reflections on the surface. Thus, the semiconductor layers produced according to the invention are particularly suitable for solar cells or photoreceivers.

In particular in its application for solar cells or photoreceivers, the porous semiconductor layer to be recrystallized can also be provided with surface texturing, in particular with a texturing such as a pyramid texture. This can either be carried out before the etching process on the crystalline starting surface or can also be incorporated in the etching processing or following the etching process. The textured surface of the manufactured crystallized semiconductor layer forms together with the enclosed voids a structure with which a high light absorption, and thus in solar cells high conversion efficiency, are to be expected.

The semiconductor layers produced according to the invention are however also suitable for other components such as transistors, in particular thin-layer transistors, micromechanical components or systems, sensors, or radiation-resistant electronic circuits.

As starting materials, other semiconductor materials such as silicon compounds or III-V compounds or II-VI compounds can also be used. For each of these materials solutions containing hydrogen fluoride can also be used experimentally as an etching solution.

Furthermore, another material, e.g. another semiconductor material, can be introduced, before the temperature treatment, into the pores open outwards at the surface of the porous layer. This can, for example, be carried out by an electrolytic process, by a vapor deposition process, or from the liquid phase. The material arising is then a mixed semiconductor or an alloy. Through the subsequent heat treatment, new materials are obtained with compositions which previously could not be obtained otherwise.

Claims

1. Process for the manufacture of a crystalline semiconductor layer (**26**), in which at least one porous

layer (21, 31) is produced at the surface of a semiconductor substrate (20, 30) and then the porous layer is removed from the semiconductor substrate and either before or after its removal is at least partially recrystallized by heat treatment.

2. Process according to claim 1, with the process steps:

a) providing a semiconductor substrate (20) with a surface,

b) producing a first porous layer (21) adjacent to the surface and with a first porosity curve in a range of relatively low porosity,

c) producing a second porous layer (22) within or adjacent to the first porous layer (21) and with a second porosity curve which at least partially lies in a range of relatively high porosity,

d) heat-treating, and thus at least partial recrystallizing, the first porous layer (21) and converting at least a part of the second porous layer into a separation layer (23),

e) removing the first recrystallized layer (26) at the separation layer (23).

3. Process according to claim 1, with the process steps

a) providing a semiconductor substrate (30) with a surface,

b) producing a first porous layer (31) adjacent to the surface and with a first porosity curve in a range of relatively low porosity,

c) producing a second porous layer (31) [sic] within the, or adjacent to the, first porous layer (31) and with a second porosity curve which is constituted in such a manner that a full-surface removal of the porous layers occurs during the process,

d) heat-treating, and thus at least partial recrystallizing, the porous layers.

4. Process according to claim 2, in which the second porous layer (22) has a relative maximum of porosity over depth.

5. Process according to claim 3, in which the second porous layer (32) has a continuous increase of porosity over depth.

6. Process according to one of the foregoing claims, in which the porous layers are produced by an electrolytic wet-etching process in which the semiconductor substrate is in contact with an electrolytic solution and is energized with an electric current.

7. Process according to claim 6, in which the electrolytic solution contains hydrogen fluoride.

8. Process according to claims 4 to 6, in which the porosity is set by the current.

9. Process according to claim 6, in which the concentration of electrical solution remains constant during the process.

10. Process according to claim 6, in which the concentration of the electrical solution is varied during the process.

11. Process according to claim 2, in which process step e) is done by the fact that a foreign substrate (25) is applied to the surface of the semiconductor substrate and the foreign substrate (25) is subsequently lifted.

12. Process according to one of the foregoing claims, in which the semiconductor substrate contains silicon, in particular consists of elemental silicon or of a silicon compound such as SiGe, SiC, or other Si-containing alloys.

13. Process according to one of claims 1 to 10, in which the semiconductor substrate consists of a III/V semiconductor, in particular of GaAs.

14. Process according to one of claims 1 to 12, in which before the etching process a macroscopic surface texturing is produced in the semiconductor layer, in particular a texture such as a pyramid texture.

15. Process according to one of claims 1 to 14, in which before the thermal expansion an additional material, in particular an additional semiconductor material, is introduced into the pores open outwards at the surface of the first porous layer (21).

16. Crystalline semiconductor layer produced according to a process according to one or more of the foregoing claims.

17. Solar cell or photo receptor comprising a crystalline semiconductor layer according to claim 16.

18. Solar cell or photo receptor according to claim 17, in which the crystalline semiconductor layer comprises voids acting as light-scattering centers.

19. Thin layer transistor, in particular for the control electronics or driver circuits for displays, comprising a crystalline semiconductor layer according to claim 16.

20. Sensor component, in particular gas sensor, comprising a crystalline semiconductor layer according to claim 16.

21. Micromechanical component or system comprising a crystalline semiconductor layer according to claim 16.

22. Integrated circuit comprising a crystalline semiconductor layer according to claim 16.

23. Radiation resistant components, circuits or systems comprising a crystalline semiconductor layer according to claim 16.

4 Page(s) of
Drawings Appended

DRAWINGS SHEET 1

Number: **DE 198 41 430 A1**
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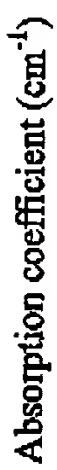
[see source for figures 1 and 4]



Photon energy (eV)

DRAWINGS SHEET 2

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[see source for figures 2a, 2b, 2c, and 2d]

DRAWINGS SHEET 3

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[see source for figures 2e and 2f]

DRAWINGS SHEET 4

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[see source for figures 3a, 3b, 3c, and 3d]